Notice of Allowability	Application No.	Applicant(s)	
	10/624,478	LIN, CHE-LI	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/19/2006*.

2. ☒ The allowed claim(s) is/are *1-12 and 14-18*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/19/2006 has been entered.

Specification

Applicant's amendment to the specification is acknowledged, where the word "integrated" is added for support in describing the invention, namely an integrated control chip. No new matter is believed to be introduced, as paragraph [0024] previously stated, "the control chip 122 is introduced to provide timing and control signals for driving and controlling the thin film transistors, and simultaneously to provide logical functions of decoding and delivering signals from the sensor board." Please see figure 3, element 122 as the figurative representation of the integrated control chip.

Allowable Subject Matter

1. Claims 1-12 and 14-18 are allowed.

2. The following is an examiner's statement of reasons for allowance:

With respect to **Claim 1**, AAPA teaches a backlight unit for a flat panel display (FPD). The AAPA teaches the backlight unit to comprise a lightguide *(figure 1, 32)*, providing light propagating paths *([0006], lines 3-4)*; a lamp *(38)*, disposed beside the lightguide to emit lights into the lightguide in an edgelight form, the lights emitted into the lightguide propagate therethrough in a total reflection form *([0006], lines 5-7)*; optical films *(34)* are disposed on the lightguide for scattering lights emitted from the lightguide uniformly *([0006], lines 1-12)*; an antenna array layer *(42)* and a reflector surface layer *(36)*, where the antenna array layer is applied to receive inputting signals from a hand-held stylus *([0007], lines 3-6)*, and the reflector surface layer is applied to reflect lights dispersed from the lower surface of the lightguide *([0006], lines 8-10)*. AAPA teaches a control circuit board, attached beneath the sensor board *([0007], lines 1-4)*, connected electrically for driving the thin film transistors via a flexible printed circuit board *([0008], lines 2-5; [0005], lines 11-17)*, and connected to the sensor board via a connecting bus for decoding the signals received by the sensor board ([0007], lines 8-11).

The AAPA teaches a sensor board *(42)* but the sensor board is not attached to a lower surface of the lightguide comprising an antenna array layer and a reflector surface layer.

Keely discloses a flat panel display in which a digitizer is integrated. Keely teaches a sensor board *(figure 1, 56 and 60)* attached to a lower surface of the lightguide *(54; column 4, lines 13-14)* comprising an antenna array layer *(60; column 4, lines 22-23)* and a reflector surface layer *(56)*. The sensor board of Keely is shown in figure 1, where the layer comprises elements 50, 54, 56, and 60.

Ahn et al. (Pub. No.: US 2002/0089492) teaches two control chips fabricated on the same circuit board to provide timing control signals for driving the thin film transistors and executing

a logical function of decoding signals from the sensor board *([0063], lines 9-15; [0064], lines 7-11)*. Although Ahn teaches two control chips coexisting on the same PCB, Ahn does not teach an integrated control chip.

None of the prior art teaches an integrated control chip fabricated on the control circuit board to provide timing control signals for driving the thin film transistors and executing a logical function of decoding signals from the sensor board.

With respect to **Claim 7**, the AAPA discloses a flat panel display. The AAPA teaches a flat panel display *(figure 1)* comprising a display module *(20)*, having a lower glass substrate *(24)* for fabricating thin film transistors *([0005], lines 12-13)*, an upper glass substrate *(22)*, a displaying molecule layer inserted between the lower glass substrate and the upper glass substrate *([0005], lines 5-6)*, where the lower glass substrate is connected electrically to one single control circuit board *([0007], lines 8-10; as shown in figure 1, element 48, only one control circuit is used for driving the transistors)* via a flexible printed circuit board for driving the thin film transistor *([0005], lines 9-13)*; a backlight unit *(30)*, fabricated beneath the display module *(20)*, having a lightguide *(32)*, a lamp disposed aside the lightguide to emit lights into the lightguide in an edgelight form *(38; [0006], lines 4-5)*, and optical films for scattering lights emitted from an upper surface of the lightguide uniformly *(34; [0006], lines 10-12)*. The AAPA teaches a sensor board for receiving inputting signals from a hand-held stylus above the flat panel display *([0007], lines 3-6)*. The AAPA teaches a reflector surface layer for reflecting lights dispersed from the lower surface of the lightguide *(36; [0006], lines 8-10)*; where the flexible printed circuit board is wound downward around a sidewall of the backlight unit to have the

single control circuit board be attached beneath the backlight unit *([0008], lines 2-4)*, where the single control circuit board is connected electrically to the sensor board via a connecting bus to decode signals received by the sensor board *([0007], lines 6-10)*.

The AAPA does not teach an upper glass substrate for fabricating a color filter. The AAPA does not teach optical films disposed on the lightguide nor does the AAPA teach a backlight unit comprising a single layer sensor board attached to the lower surface of the lightguide where the sensor board comprises a reflector surface layer.

Keely discloses a flat panel display in which a digitizer is integrated. Keely teaches an upper substrate for fabricating a color filter *(figure 7, upper substrate ~front glass (34), color filter (130))*. Keely teaches optical films *(figure 1, 50)* disposed on the lightguide and a backlight unit comprising a sensor board *(figure 1,56 and 60)* attached to the lower surface of the lightguide *(figure 1, lightguide~lightpipe; column 4, lines 14-15)* where the sensor board comprises a reflector surface layer *(56)*. Keely teaches a single layer sensor board *(figure 1, 56 and 60)* attached to a lower surface of the lightguide *(54; column 4, lines 13-14)* comprising an antenna array layer *(60; column 4, lines 22-23)* and a reflector surface layer *(56)*. The single layer sensor board of Keely is shown in figure 1, where the layer comprises elements 50, 54, 56, and 60.

Ahn et al. (Pub. No.: US 2002/0089492) teaches two control chips fabricated on the same circuit board to provide timing control signals for driving the thin film transistors and executing a logical function of decoding signals from the sensor board *([0063], lines 9-15; [0064], lines 7-11)*. Although Ahn teaches two control chips coexisting on the same PCB, Ahn does not teach an integrated control chip.

None of the prior art teaches an integrated control chip fabricated on the control circuit board to provide timing control signals for driving the thin film transistors and executing a logical function of decoding signals from the sensor board.

With respect to **Claim 14**, the claim differs from claim 7 only in that the limitation "wherein said flexible printed circuit board is wound downward around a sidewall of said backlight unit to have said control circuit board be attached beneath said backlight unit, wherein said control circuit board is connected electrically to said sensor board via a connecting bus to decode signals received by said sensor board" is recited in claim 7 and claim 14 recites the limitation "a liquid crystal molecule layer, disposed between said upper glass substrate and said lower glass substrate" and "one single control circuit board, attached beneath said sensor board". The AAPA teaches a liquid crystal molecule layer, disposed between said upper glass substrate and said lower glass substrate *([0005], lines 5-7)*. Since the backlight unit comprises a single layer sensor board, as discussed in claim 7, then the control unit is attached beneath the sensor board as well.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
SUPERVISORY PATENT EXAMINER